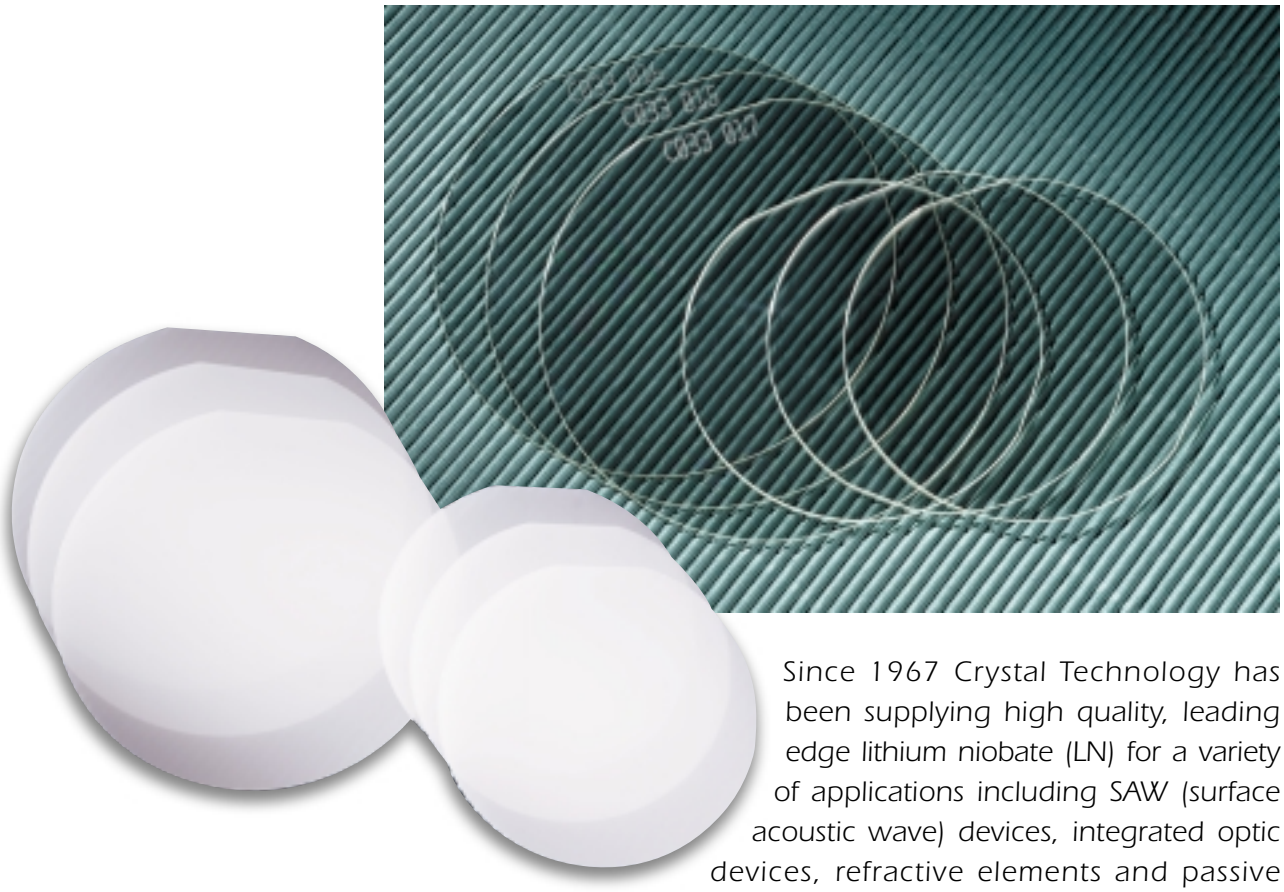
Lithium Niobate

application note – single crystal substrates



Since 1967 Crystal Technology has been supplying high quality, leading edge lithium niobate (LN) for a variety of applications including SAW (surface acoustic wave) devices, integrated optic devices, refractive elements and passive detectors. As a world leader in lithium niobate we are committed to continuously improving the quality of LN to meet the ever increasing performance demands of these technologies.

Crystal Technology, Inc.
An EPCOS Company

In this application note, we discuss various issues that may prove useful to customers involved in processing lithium niobate (LN) single crystal substrates. They reflect common concerns and questions we have encountered from existing customers using LN in a variety of applications. The discussion is divided into the following sections:

- Handling
- Cleaning
- Surface Quality
- Wafer Flatness
- Crystal Polarity

HANDLING

As is the case with most substrate materials used in device manufacture, operators should take the precautions of using gloves and vacuum wands when handling LN substrates. The plastic shipping containers, either individual carriers or boats of up to 25 wafers, should be sealed at all times and opened only under a flow hood or in a clean-room environment. In addition to these considerations, there are a few properties specific to LN of which all personnel involved in its handling should be made aware.

1) LN is a brittle material. Our edge-grinding process minimizes chipping and cracking by producing a smooth radius on the wafer's edge, and for other geometry's edge bevels can serve the same function. However, care must still be taken to avoid rough handling or impact of any kind to LN substrates. Vacuum wands or tweezers should ideally be made of relatively soft non-metallic materials. This applies as well to any carriers or boats used in wafer processing equipment.

2) LN is both pyroelectric and piezoelectric, and therefore generates an electrical potential when either thermally cycled or mechanically stressed. Since thermal cycling is virtually unavoidable during device manufacturing, it is important to be aware of the effects of these properties. Most importantly, build-up of static charge on the wafer causes it to act as a 'dust magnet', and special care must be taken to maintain a particulate-free environment during and after thermal processing. Such charges may also create mechanical strains in the crystal, and thereby increase the risk of wafer breakage. Thermal shock should be avoided by allowing for gradual heating and cooling ramps (as a rule of thumb, we recommend ~1 degree Celsius/minute). In routine processing the piezoelectric properties of LN shouldn't present a problem, as long as the wafer is not squeezed excessively in fixturing or during handling.

CLEANING

In standard volume wafer production, CTI uses either cassette-to-cassette automated wafer scrubbing or sonic batch cleaning. In the scrubbers, the wafer surface is sprayed with an ammonia-based cleaning solution, scrubbed by soft nylon bristle rollers, then rinsed in D.I. water and spin-dried under a dry nitrogen air-jet. Sonic batch cleaning uses first an ultrasonic bath to remove the larger particulates (>10µm), then a megasonic bath to remove the smaller particulates (<10µm), followed by an isopropyl alcohol dry.

For routine hand-cleaning of parts, we recommend immersion in a solution of soapy water with a pH between 7.0 and 8.5 or low concentration ammonia in water, followed by hand-wiping with undenatured ethyl alcohol, or, in a mixture of four parts alcohol and one part acetone. Using a litho-pad, lens tissue, or cotton swab, the hand-wiping should always occur in a continuous motion from one edge to the other to avoid leading- or trailing-edge stains.

Throughout any cleaning process, manual or otherwise, it is critical to avoid letting the wafer dry during intermediary steps or prior to the final drying step. Premature drying leaves stains or residue from the baths or cleaning solutions that can be difficult to remove. Parts should be moved directly from bath to bath and should not sit out in open air prior to the final drying step, whether that is spin-drying, vapor degreasing, or manual blow-drying.

SURFACE QUALITY

The U.S. Military Surface Quality Specification, MIL-O-13830A, is a standard for the specification of surface quality in optical components. This standard is used at CTI to specify various levels of surface quality in our products, and is commonly referred to as 'scratch-dig'. We compare our products with scratch and dig standards manufactured according to U.S. military drawing C7641866 Rev L, and our inspection areas are equipped with lighting which meets the standard's requirements.

In the scratch-dig system, a given quality level is expressed as two numbers—the first specifies the maximum allowable width of scratches, and the second specifies the maximum allowable diameter of digs, or pits. Typical scratch-dig numbers used at CTI range from 10-5 to 60-40, and specify defect size limits as shown in Table 1.

With respect to individual scratches or digs that exceed these requirements, the scratch-dig specification is straightforward and simple to interpret. For a 20-10 specification, the presence of any scratch greater than 2 microns in width, or any single dig greater than 100 microns in diameter, would be cause to reject or rework a part.

However, on parts where one or more defects are present which are equal to or less than the maximum allowable width or diameter, scratch-dig provides criteria for limiting the accumulation of scratches or digs proportional to the surface area being inspected.

When maximum scratches (equal to the maximum allowable width) are present, the combined length may not exceed one quarter the 'computing diameter' (which is the diameter of a circle of equivalent area to the surface being inspected). Secondly, when a maximum scratch exists along with smaller scratches, the sum of the products of the scratch numbers times the ratio of their length to the computing diameter of the inspected surface shall not exceed the maximum scratch number.

With respect to digs, maximum size digs (equal to the maximum allowable diameter) cannot exceed one per every 20 millimeters of computing diameter. Also, the sum of the diameters of all digs may not exceed twice the diameter of the maximum size specified per 20 millimeters of computing diameter.

The scratch-dig standard inevitably involves some subjectively in determining sizes of various defects, but CTI strives to maintain consistent inspection methods through periodic audits and re-training of our skilled inspectors.

Scratch #	Max width (in microns)	Dig #	Max diameter (in microns)
10	1	5	50
20	2	10	100
40	4	20	200
60	6	40	400

TABLE 1. SCRATCH-DIG

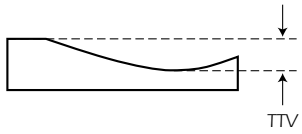
WAFER FLATNESS

Flatness is a critical parameter in many applications for LN wafers, particularly those involving the photolithography of fine structures (<1 micron). CTI employs an automatic wafer flatness tester which provides extensive sorting capabilities (cassette to cassette) as well as complete topographical analysis of the surface of a given wafer. This non-contact, grazing incidence interferometer uses a computer to analyze reflected fringe patterns and reconstruct the wafer topography mathematically. Because of the oblique angle of incidence of the laser source, the machine is capable of measuring as-cut or lapped surfaces as well as polished surfaces.

Wafers can be sorted by a variety of flatness parameters, both clamped (using a vacuum chuck) and unclamped (free-state). Clamped parameters include total indicated reading (TIR), total thickness variation (TTV), and taper. Unclamped parameters include warp and bow. Figure 1 provides definitions for each of these.

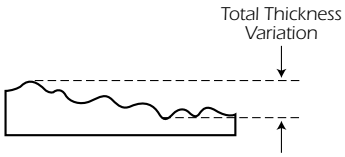
For standard wafers, CTI specifies clamped wafer flatness by TTV alone. This also allows customers the opportunity to verify flatness on wafers using a digital micrometer and the five point measurement method for gauging total thickness variation as described in ASTM standard F533. For specifying free-state flatness in standard wafers, warp alone is used, since the bow parameter as defined here is primarily used to describe the direction of curvature but not the overall magnitude.

Flatness on the surfaces of non-wafer geometry's of LN (blocks, plates) are measured with an interferometer. Flatness is expressed in fraction of the wavelength of the incident light, 633 nm.



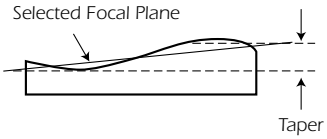
TOTAL THICKNESS VARIATION (TTV)

The difference between the highest and lowest point on the top surface of the wafer.



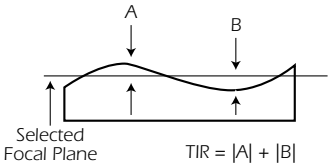
LOCAL THICKNESS VARIATION (LTV)

A stepper exposure simulation measures the difference between the highest and lowest point on the top surface of the wafer for each exposure site. Results can be reported as the maximum value found for each wafer or the percent exposure sites under a given LTV value. Common site areas used are 5x5mm and 10x10mm.



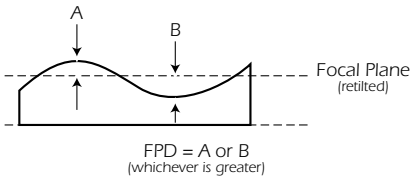
TAPER

The lack of parallelism between the back surface of the wafer and the selected focal plane (best fit plane). The value reported is the amount of rise in the focal plane, not the slope of the surface, and is therefore expressed in microns for the entire given diameter.



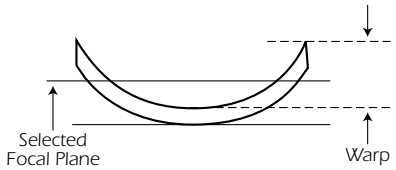
TOTAL INDICATED READING (TIR)

The difference between the highest and lowest point on the wafer surface measured normal to the selected focal plane. This essentially removes overall taper of the wafer from the measurement.



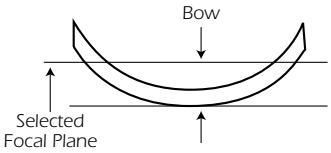
FOCAL PLANE DEVIATION (FPD)

The greatest distance above or below the selected focal plane (best fit plane). Measurements are reported as positive or negative, whichever is greater.



WARP

The difference between the highest and lowest point on the wafer surface measured normal to the selected focal plane in the free state.



BOW

The difference between the selected focal plane and the surface of the wafer at the center in the free state. This value can be positive or negative.

FIGURE 1. FLATNESS PARAMETER DEFINITIONS

CRYSTAL POLARITY

Many LN applications call for the specification of electrical polarity of the various faces of the fabricated substrate. Our convention for specifying and measuring LN crystal polarity is based on the standard method described by R.S. Weiss and T.K. Gaylord in the article titled "Lithium Niobate: Summary of Physical Properties and Crystal Structure," Applied Physics A 1985, p. 192. Upon heating or compression of lithium niobate across the c axis, the lithium and niobium ions move closer to their centered (paraelectric) positions relative to the oxygen layers of the unit cell. This reduced net polarization allows a compensating buildup of electrons on the plus face, causing it to become negatively charged.

Accordingly, LN polarity is determined by measuring the charge generated from heating or squeezing a part with a micro-voltmeter. The deflection of the needle (positive or negative) indicates the polarity of a given face. In practice, we have found that heating the crystal, as opposed to squeezing it, provides the least ambiguous result and the least potential for damaging polished surfaces.

The diagram in figure 2 shows the measurement apparatus. A flat clean conductive surface can serve as the bottom electrode, and a small square of conductive foil as the top electrode. Use a heat gun (or a blow-dryer) to gently heat the wafer and take note of the needle deflection. If you choose to use the compression method instead, use a pencil eraser or similar soft instrument to apply a gentle, increasing pressure over the top foil electrode.

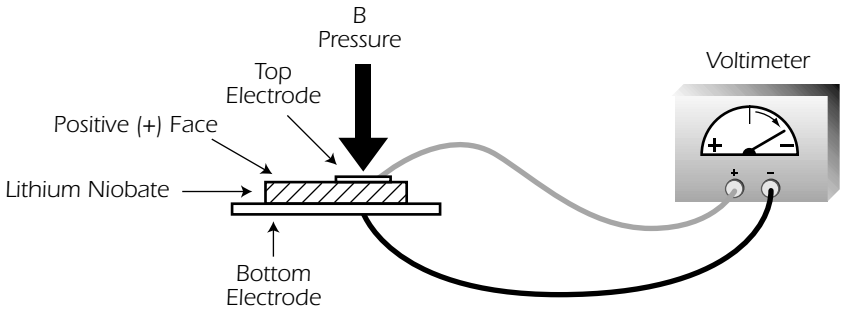


FIGURE 2. CRYSTAL POLARITY MEASUREMENT

References

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[2] Young and Yao, "Design Consideration for Acousto-optic Devices, " Proceedings of IEEE, vol. 69, no. 1, pp. 54-64 (January 1981)

[3] Richard V. Johnson, " Temporal Response of the Acousto-optic Modulator in the High Scattering Efficiency Regime", Applied Optics, vol. 18, pp. 903-907 (March 1979)

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